In claim 37, line ~~13~~ 12, following the word "electrode", - - is formed of a single conductive layer including a first portion formed over the via – level intermetal dielectric and a second portion which - - was inserted.

7/9/07

Allowable Subject Matter

5. Claims 16 – 29, 31 and 33 – 37 are now allowed.

6. The following is an examiner's statement of reasons for allowance:

Claims 16 – 29, 31 and 33 recite, inter alia, metal – insulator – metal capacitor, the structure comprising a line trench extending substantially completely through the trench – level intermetal dielectric to contact the via – level intermetal dielectric, a via extending through the via – level intennetal dielectric without extending through the trench – level intennetal dielectric and a metal – insulator – metal capacitor formed between the via – level intermetal dielectric and the trench – level intermetal dielectric to include a lower electrode, a dielectric layer, and an upper electrode. The art of record does not disclose or anticipate the above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Claims 34 – 36 recite, inter alia, a dual damascene interconnection structure with a metal – insulator – metal capacitor, the structure comprising a via – level intermetal dielectric and a trench – level intermetal dielectric and a metal – insulator – metal capacitor formed between the via – level intermetal dielectric and the trench – level intermetal dielectric and an alignment key formed only in the via – level intemaetal dielectric so as to have the step difference to align the metal – insulator – metal